Remarks:

Reconsideration of the application is requested.

Claims 1-16 remain in the application. Claims 10 and 11 have been amended. Claims 1-9 have been withdrawn from consideration.

In item 1 on page 2 of the above-identified Office action, claims 10, 11, and 16 have been rejected as being obvious over *Forbes et al.* (US 6,498,065) in view of *Fitch et al.* (US 5,554,870) and further in view of *Burns, Jr. et al.* (US 6,077,745) under 35 U.S.C. § 103.

The above-noted rejection and the Examiner's comments have been considered. Consequently, claim 10 has been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found in claim 11 as originally filed.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 10 as amended calls for, inter alia:

> A vertical semiconductor transistor component, comprising:

> vertical pillar structures ..., said vertical pillar structures having respective base sides, circumferential wall regions, and capping sides, said vertical pillar structures ***being formed by using a statistical mask;***

The inventive concept of the invention of the instant application is to define the channel length of the vertical semiconductor transistor component by a layer-producing step, while defining the channel width, independently of the lithography, by a statistical mask. According to the specification on pages 6-7: "The combination of these two principles (definition of all the individual channel lengths by a common layer-producing step and definition of the individual channel widths by a statistical mask) makes it possible to produce a short-channel FET with small individual channel widths and also makes possible a substantially complete punchthrough of the potential generated by the second electrical contact (gate) through the individual channels, whereby effective transistor control is made possible and parasitic short-channel effects are eliminated."

In pages 2-3 of the Office action, the Examiner stated:

> Regarding Claims 10,11, and 16, Forbes et al. disclose a memory address decode array with vertical transistors where a decoder for a memory device is provided. The decoder array includes a number of address lines and a number of output lines. The address lines and the output lines form an array. A number of vertical transistors are selectively

> disposed at intersections of output lines and address lines. Each transistor is formed in at least one pillar of semiconductor material that extends outwardly from a working surface of a substrate. The vertical transistors each include source, drain, and body regions. A gate is also formed along at least one side of the at least one pillar and is coupled to one of the number of address lines. The transistors in the array implement a logic function that selects an output line responsive to an address provided to the address lines. Forbes et al. fail to disclose the required capping layer and insulators and the pillar in the required manner. However, Fitch et al. disclose an integrated circuit having both vertical and horizontal devices and process for making the same where the required capping layer is disclosed. Furthermore, Bums, Jr. et al. disclose a self-aligned diffused source vertical transistors with stack capacitors in a 4F-Square memory cell array where the required insulators and pillars in the required manner is disclosed.
>
> It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required capping layer and the insulator and pillar in the required manner as taught by Fitch et al. and Burns, Jr. et al. respectively in order to have a vertical memory structure with better performance.

However, the Examiner did not address the use of a statistical mask. *Forbes et al.* do not contain the word "statistical", or related words.

A *product-by-process* limitation does not by itself have any patentable weight in a product claim since it is the final device structure which carries weight for patentability purposes. However, a *product-by-process* limitation has patentable weight in a product claim if it results in a structurally distinct product and if the nature of the structural distinction is not known or cannot be easily

recited in the claims. This is believed to be the case in the invention of the instant application. Forming the vertical pillar structures using a statistical mask results in a structurally different product whose precise structural distinction can not be easily recited in the claim, and therefore, it is believed that the *product-by-process* limitation recited in claim 10 must be given patentable weight.

Consequently, the invention as recited in claim 10 of the instant application is believed not to be obvious over *Forbes et al.* in view of *Fitch et al.*, and further in view of *Burns, Jr. et al.*.

It is accordingly believed to be clear that *Forbes et al.* in view of *Fitch et al.*, and further in view of *Burns, Jr. et al.*, do not suggest the features of claim 10. Claim 10 is, therefore, believed to be patentable over the art and because claims 11-16 are ultimately dependent on claim 1, they are believed to be patentable as well.

Considering the deficiencies of *Forbes et al.*, it is believed not to be necessary at this stage to address the secondary references *Fitch et al.* and *Burns, Jr. et al.*, or the secondary references applied in the rejection of dependent claims 12-15 in items 2-4 of the Office action, and whether or

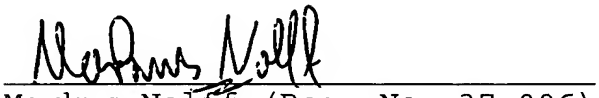
not there is sufficient suggestion or motivation with a reasonable expectation of success for modifying or combining the references as required by MPEP § 2143.

In view of the foregoing, reconsideration and allowance of claims 10-16 are solicited.

If an extension of time is required, petition for extension is herewith made.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,



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